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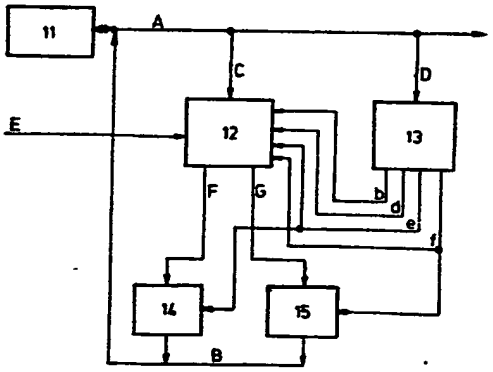
(57) Abstract



In the course of the procedure the time interval between two successive signal changes is determined and possibly stored in such a way, that the time interval measured between the last two signal changes is compared with the previously stored minimum value, and at the same time with a minimum limit postulated and stored beforehand; the value of time interval just measured will only be stored as the new minimum value, if it is less than the previously stored one, but at the same time it is greater than the postulated minimum limit (in this case the previously stored minimum value will be lost); and/or in the course of the comparisons it will be investigated, whether the value lastly measured is greater than the previously stored maximum value, and at the same time, it is less than the maximum limit postulated and stored beforehand, and thereafter the new value will only be stored as the new maximum value, if the above conditions are fulfilled (in this case however, the previously stored maximum value is lost). The invented device comprises a control unit (11), an address decoder unit (13), a first gating unit (14), a baud-rate and signal distortion detector unit (12) and a second gating unit (15). The inputs of the baud-rate and signal distortion unit (12) are connected via the first addressing line (b) and via the second addressing line (d) to the respective outputs of the address decoder unit (13), another input via the third addressing line (e) to a further output of the address decoder unit (13) and to an input of the first gating unit (14), a further input via the fourth addressing line (f) to a further output of the address decoder unit (13) and to an input of the second gating unit (15), further inputs of it to the group of input data lines (E) constituting the input of the device, the remaining inputs via the group of writing lines (C), being a subset of the group of central lines (A) to the inputs/outputs of the control unit (11); the outputs of the baud-rate and signal distortion detector unit via the first bunch of data lines (F) to the further inputs of the first gating unit (14), via the second bunch of data lines (G) to the further inputs of the second gating unit (15). The outputs of the first gating unit (14) are applied via the group of reading lines (B) constituting a part of the group of central lines (A) to the inputs/outputs of the control unit (11) and to the outputs of the second gating unit (15).

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PROCEDURE AND DEVICE TO DETERMINE DATA TRANSMISSION RATE AND SIGNAL DISTORTION OF SYNCHRONOUS AND ASYNCHRONOUS SERIAL DATA TRANSMISSION LINES

FIELD OF THE INVENTION

THe Subject of the invention is a procedure and a device to determine any or both of data tras,ission rate and signal distortion of serial data transmission lines.

As it is well-known information exchange between various data processing equipments, computers, terminals, being interconnected by mutual data communication is realized in teh majority of cases by synchronous and/or asynchronous serial data transmission using local or remote data transmisson lines.

A need has arisen that data processing equipment (which may be for example a line multiplexer, a front-end processor, an intelligent line switching and data processing system, etc) receiving and pre-processing input data be able to carry out baud rate and/or protocol-conversion and transmit data to a central processing unit, be suitable for monitoring input SERiAL DATA AND PROVIDING INFORMATION ON DATA TRANSMISSION rate and distortion (jitter, skew). Characteristic of known solutions and equipment is that data transmission rate and signal distortion is measured and determined by two different circuits or devices, being independent of each other, and because known circuits for determining signal distortion are relatively complicated, in most cases distortion will only be measured, if it is absolultely indispensable.

The main point of the known methods for determining data transmission rate of an asynchronous serial data stream is that the length of the START bit of the first (or the first two) transmitted characters (that is the time interval extending from the leading edge of the START bit until the next strailing edge in the serial data stream) is determined, and from this value, taken as a unity bit time, can be concluded on the actual data rate.

Data rate, calculated in such a way, is regarded as valid hereafter for the whole data transmission.

The disadvantages of the above simple method are the following:

- The first (first two) character, to be sent out at the beginning of the data stream cannot be chosen arbitrarily, in most cases only a Carriage Return is allowed. Namely, if the value of the LSB bit (the first data bit after START in the serial bit stream) of the character being examined is not a logical "1", the first signal change will not occur in a unity bit time interval after the leading edge of the START bit, hence the above measurement will result in an erroneous value.

- Using the above method, data rate cannot be measured in course of data transmission, that is after the first (appropriately chosen) character(s) have been transmitted. However, this would be desirable for example if the line is "listened to" by a protocol analyzer.

- Although the exact value of the length of the START bit determined by using the above method depends on the signal distortion, and therefore it should be rounded (that is: corrected), the information gained in such a way is not enough to determine the exact value of the signal distortion.

In order to gain information about signal distortion, generally the following known method is applied. The distorted signal is regenerated, then the regenerated and the distorted signal is sampled in several moments in time, these moments being measured relative to the beginning of the regenerated signal in terms of the percental value of the bit time. Corresponding pairs of sampled values are compared and the time moments are searched, at which the two corresponding samples differ from each other. The percentage values determined in such a way are considered as characteristic of the signal distortion.

The above method is applied for example in the Telex and Data Switching System type NEDIX-510A of Nippon Electric Corporation (Japan).

Disadvantages of the above method are the following:

- the method necessarily implies signal regeneration, which may only be realized by a relatively complicated circuit itself;

- the multiple sampling, the generation of various sample-time positions, etc. require relatively complicated circuits, nevertheless the result of this measurement will only be characteristic of the sampled bit, not of the whole serial data stream.

SUMMARY OF THE INVENTION

By reason of the difficulties, outlined above, the aim of the invention is to develop a device, which

- enables data transmission rate and distortion to be measured by aplying a single, homogeneous method;

- measures and determines data rate and distortion continously, therefore the measured values can be read out and evaluated in any phase (that is: not only at the beginning) of the data transmission;

- with respect to measuring data rate, imposes no constraints, or at least far less contraints on the transmitted characters to be measured;
- enables the input data stream to be analized with respect to signal distortion in detail, without requiring signal re-generation.

The basis of the invention is the perception, that the task can easily be solved, if bit time minimum and bit time maximum values are continuously and concurrently measured and determined in the course of the whole data transmission.

The procedure according to the invention is an improvement of a known procedure in the course of which at first signal changes are indicated, then the time interval between two succesive signal changes aredetermined and stored.

The improvement lies in that saidtime intervals are continuously measured and the time interval measured between the last two considered signal changes is compared with a previously stored minimum value, and at the same time with a minimum limit postulated and stored beforehand; the value of time interval just measured will only be stored as a new minimum value, if it is less than the previously stored one, but at the same time it is greater than the postulated minimum limit (in this case the previously stored minimum value will be lost); and optionally in the course of the comparisons it will be investigated, whether the value last measured is greater than the previously stored maximum value, and at the same time, it is less than the maximum limit postulated and stored beforehand, and thereafter the new value will only be stored as a new maximum value, if the above conditions are fulfilled (in this case however, the previously stored maximum value will be lost).

Practically in the course of the invention, at the beginning of a measuring sequence the maximum value that may theoretically be stored is taken and at the examination of the first measured value it is considered as the previously measured minimum value; and similarly, the minimum absolute value, that may be stored (in practice: zero) is taken and at the examination of the first measured value it is considered as the previously measured maximum value.

The invented device is an improvement of a known device, which comprises a control unit, an address decoder unit, a baud-rate detector unit and a first gating unit, all of them connected to a group of central lines.

The improvement lies in that the device also includes a second gating unit, and instead of a baud- rate detector unit, it comprises a baud-rate and signal distortion detector unit. The inputs of said baud-rate and signal distortion detector unit are connected via a first addressing line and via a second addressing line to respective outputs of said address decoder unit, another input via a third addressing line to a further output of said address decoder unit and to an input of said first gating unit, a further input via a fourth addressing line to a further output of said address decoder unit and to an input of said second gating unit, further inputs of it to a group of input data lines constituting the input of the device, the remaining inputs via a group of writing lines being a subset of a group of central lines to the inputs outputs of said control unit; the outputs of said baud-rate and signal distortion detector unit via first bunch of data lines to further inputs of said first gating unit, via second bunch of data lines to further inputs of said second gating unit. The outputs of said first gating unit are applied via a group of reading lines constituting a part of a group of central lines to inputs/outputs of said control unit and to outputs of said second gating unit.

In the sense of the invention, the baud-rate and signal distortion detector unit suitably comprises a time marker circuit, a counter, a minimum limit register, a maximum limit register, a first comparator circuit, a second comparator circuit, a third comparator circuit, a fourth comparator circuit, a first gating circuit, a limited minimum register, a second gating circuit and a limited maximum register.

Inputs of said time marker circuit are connected to a group of input data lines, another input of said circuit is connected via a third transit line to an input of said first gating circuit and to the output of said first comparator circuit. The outputs of said time marker circuit are applied via an enabler line to an input of said counter, via a reset line to another input of said counter, via a write line to an input of said first gating circuit, and to an input of said second gating circuit, respectively. A further input of said counter is connected to a synchronizer line, constituting part of a group of central lines. The outputs of said counter are applied via a group of internal data lines to inputs of said first, second, third and fourth comparator circuits, furthermore to inputs of said limited minimum register and to those of said limited maximum register. The inputs of said minimum limit register are connected partly to a first addressing line, partly, via a group of data lines, being a subset of a group of central lines to inputs of said maximum limit register. The outputs of said minimum limit register is applied via a first group of transit lines to further inputs of said first comparator circuit. A further input of said maximum limit register is connected to a second addressing line, its outputs are applied via a second group of transit lines to further inputs of said second comparator circuit. A further input of said first gating circuit is applied via a fifth transit line to the output of said third comparator circuit, its output is connected via a first transit line to a further input of said limited minimum register. Further input of said limited minimum register is connected to a third addressing line, its outputs are connected via a first bunch of

data lines to further inputs of said third comparator circuit. Further inputs of said second gating circuit are connected via a fourth transit line to the output of said second comparator circuit, and via a sixth transit line to the output of said fourth comparator circuit respectivel The output of said second gating circuit is applied via a second transit line to an input of said limited maximum register. A further input of said limited maximum register is connected to a fourth addressing line, its outputs are connected to a second bunch of data lines, and via the second bunch of data lines to further inputs of said fourth comparator circuit.

In particular, said time marker circuit is suitably a signal change indicator circuit, consisting of edge-triggered monostable multivibrators.

Furthermore, it is also considered a practical version of said time marker circuit, in that said time marker circuit includes a first signal change indicator circuit, a second signal change indicator circuit and a storage.

The input of said first signal change indicator circuit comes from a first input data line, being part of said group of input data lines, its output is applied via a transit data line to the input of said storage. The input of said second signal change indicator circuit is connected to a second input data line, also being part of said group of input data lines, the outputs of said second signal change indicator circuit is partly connected via said reset line to a further input of said storage, partly to said write line, respectively. The output of said storage is applied to said enabler line.

It is also considered a practical embodiment of said time marker circuit, in that said time marker circuit comprises a signal change and start/stop bit indicator circuit and a bistable multivibrator.

The input of said signal change and start/stop bit indicator circuit is connected to an input data line, being part of said group of input data lines, its outputs are connected partly via a reset line to an input of said bistable multivibrator, partly via a stop signal line to another input of said bistable multivibrator, and partly to said write line, respectively. The output of said bistable multivibrator is connected to said enabler line.

In a further, suitable embodiment said time marker circuit comprises a signal change and start bit indicator circuit, a bistable multivibrator circuit and an AND gate.

The input of said signal change and start bit indicator circuit is connected to said input data line, being part of said group of input data lines, the outputs are connected partly to said reset line and via said reset line to an input of said bistable multivibrator circuit, partly to said write line and via said write line to an input of said AND gate. Another input of said AND gate comes from said third transit line, its output is connected via a stopping line to another input of said bistable multivibrator circuit. The output of said bistable multivibrator circuit is connected to said enabler line.

BRIEF DESCRIPTION OF THE DRAWINGS

Hereinafter the invention will be explained with reference to the drawings, which represent some feasible embodiment of the invented procedure and device.

In the drawings

fig. 1 is a flowchart, illustrating the invented procedure;

fig. 2 is a block diagram, illustrating the known and invented device;

fig. 3 is a block diagram illustrating possible embodiments of said baud-rate and signal distortion detector circuit;

fig. 4 is a block diagram, illustrating a possible embodiment of said time marker circuit;

fig. 5 is a block diagram, illustrating another possible embodiment of said time marker circuit;

fig. 6 is a block diagram, illustrating a further possible embodiment of said time marker circuit.

In the figures the same details are designated with the same character symbols (letters or numbers). If same or similar details appear repeatedly in one and the same figure, or if a specific detail consists of many further components, the reference numbers are supplemented with letters, the reference letters are supplemented with numbers in order to identify these particulars unambiguously. In the figures, arrows represent unidirectional, twofold and oppositely directed arrows symbolize bidirectional relations.

Referr ing to Fig. 1, the procedure is visualized by a flow-chart. The procedure starts at first time interval T1, in which the maximum value that theoretically can be stored is taken and stored as the minimum value, and furthermore, the value of the minimum limit is defined and stored. First time interval T1 is then followed by second time interval T2, in which the minimum value, that theoretically can be stored is taken and stored as the maximum value, and furthermore, the value of the maximum limit is defined and stored. Second time interval T2 is followed by third time interval T3, in which time measuring (counting) is stopped and time value is set to zero. Third time interval T3 is followed by first time moment t_1. At first time moment t_1 it is decided, if on the considered input line a logical signal change has occured, or not. If it has, first time moment t_1 is followed by second time moment t_2,if not, first time moment t_1 follows again. At second time moment t_2 it is decided, if time has to be measured continously (bit-by-bit, that is: between every consecutive signal change or by sections (that is: between given peculiar signal changes, regerded as start and stop signal edges, ignoring any other signal changes between them). If time is to be measured by sections, second time moment t_2 is followed

by third time moment t_3; if time has to be measured continously, second time moment t_2 is followed by fourth time interval T4. At third time moment t_3 it is invenstigated, if signal change, detected at first time moment t_1 is to be regarded as a start signal edge (for example, a leading edge of the START bit of an asynchronous serial character, detected by a START-bit indicator circuit, see fig. 5 and 6), or not. If it is a start signal edge, third time moment t_3 is followed by fourth time interval T4, otherwise it is followed by first time moment t_1. In fourth time interval T4 previous time value is cleared (that is: time is set to zero). Fourth time interval T4 is then followed by fifth time interval T5. In time interval T5 time measuring (time counting) is started, T5 is then followed by fourth time moment t_4. At fourth time moment t_4 it is investigated, if on the considered input line (since the last invenstigation) a logical signal change has occured or not. If it has, t_4 is followed by fifth time moment t_5, otherwise fourth time moment t_4 follows again. At fifth time moment t_5 it is invenstigated, if time has to be measured continously or by sections. If time is to be measured continously, t_5 is followed by seventh time moment t_7, if it has to be measured by sections, sixth time moment t_6 follows. In sixth time moment t_6 it is investigated, if the signal change, detected at fourth time moment t_4, is a stop signal edge, or not. If it is, (for example, it is the leading edge of the STOP bit of an asynchronous serial character, see device on fig. 5; or it is a signal change immediately following a minimum time limit value, see device on fig.6), sixth time moment t_6 is followed by sixth time interval T6; otherwise it is followed by seventh time interval T7. In sixth time interval T6 it is stored (memorized), that the last signal change was a stop signal edge. T6 is followed by seventh time moment t_7. In the seventh time interval T7 it is stored (memorized), that the last signal change was not a stop signal edge. T7 is also followed by seventh time moment t_7. In seventh time moment t_7 it is examined, whether the time value, measured (counted) until the last signal change, is greater than value of the minimum limit, defined and

stored in first time interval T1. If it is, t_7 is followed by eighth time moment t_8; if it is not, t_7 is followed by ninth time moment t_9. In eighth time moment t_8 it is examined, whether the time value measured (counted) until the last signal change is less than the minimum value stored previously. If it is, t_8 is followed by eighth time interval T8, if it is not, ninth time moment t_9 follows. In eighth time interval T8 the time value being just measured is stored as the actual minimum value (the value that was stored before is lost). T8 is followed by ninth time moment t_9, at which it is examined, whether the time value, measured (counted) until the last signal change is less than value of the maximum limit, defined and stored in second time interval T2. If it is, t_9 is followed by tenth time moment t10, if not, it is followed by eleventh time moment t11. At tenth time moment t10, it is examined, if time value measured until the last signal change is greater than the previously stored maximum value. If it is, t_{10} is followed by ninth time interval T9, if it is not, it is followed by eleventh time moment t_{11}. In time interval T9 the time value being just measured is stored as the actual maximum value (the value being stored before is lost). T9 is followed by eleventh time moment t_{11}. At eleventh time moment t_{11} it is examined once more, if time has to be measured continously or by sections. If it is to be measured continously, t_{11} is followed by tenth time interval T10, if it has to be measured by sections, twelfth time moment t_{12} follows. In tenth time interval T10 actual time value is set to zero, however time measuring (counting) is not stopped. T10 is then followed by fourth time moment t_4 again. At twelfth time moment t_{12} it is examined, whether the last signal change was a stop signal edge (this condition has been stored in sixth time interval T6 that is in seventh time interval T7).
If it was, t_{12} is followed by third time interval T3, if it wasn't fourth time moment t_4 follows. The whole procedure goes on cyclically until time measuring is stopped.

The operation of a known baud-rate detection device will be explained with reference to fig. 2.

The device comprises a control unit 11, an address decoder unit 13, a baud-rate detector unit 12 and a first gating unit 14. An input of said baud-rate detector unit 12 are connected via first addressing line b to the output of said address decoder unit 13. Further inputs of said baud-rate detector unit is connected to a group E of input data lines, constituting the input of the device, its outputs are applied via a first bunch E of input data liens to the inputs of said first gating unit 14. A further input of said first gating unit 14 is connected via a third addressing line e to a further output of said address decoder unit 13, the outputs of said first gating unit 14 are applied via a group B of reading liens constituting a subset of a group A of central lines to inputs/outputs of control unit 11. The inputs of said address decoder unit 13 are connected to a group D of address and central lines, being a subset of a group A of central lines, and being connected to inputs/outputs of control unit 11.

Said baud-rate detector unit 12 receives via a group E of input data lines a serial input data stream (that is: a series of input signal pulses). When said baud-rate detector unit 12 receives a pulse via said first addressing line b (this pulse is generated by said address decoder unit 13 if so instructed by said control unit 11 via said group A of central lines), said baud rate detector unit 12 generates a binary value being characteristic of the time interval between two consecutive signal changes just appearing on an appropriate line of said group E of input data lines. This value, being characteristic of said time interval (which in turn, on certain afore-mentioned conditions characterizes transmission rate of the serial input data stream), appears on outputs of said baud-rate detector unit 12, and in such a way, on said first bunch F of data lines. This value is then gated by said first gating unit 14 onto said group A of central lines, when a pulse is generated onto said third addressing line e by said address decoder unit 13. Data appearing on said group A of central lines may then be processed by said control unit 11.

The invented device will also be explained with reference to fig.2.

The device according to the invention differs from that of the known solution in that it also includes a second gating unit 15, and instead of a baud-rate detector unit, it comprises a baud-rate and signal distortion detector unit 12. The inputs of said baud-rate and signal distortion detector unit 12 are connected via a first addressing line b and via a second addressing line d to respective outputs of said address decoder unit 13, another input of it via a third addressing line e to a further output of said address decoder unit 13 and to an input of said first gating unit 14, a further input via a fourth addressing line f to a further output of said address decoder unit 13 and to an input of said second gating unit 15, further inputs of said baud-rate and signal distortion detector unit 12 to a group E of input data lines constituting the input of the device; the remaining inputs of it via a group C of writing lines being a subset of said group A of central lines to inputs/outputs of said control unit 11; and to inputs of said address decoder unit 13; outputs of said baud-rate and signal distortion detector unit 12 via a first bunch F of data lines to further inputs of said first gating unit 14, via a second bunch G of data lines to further inputs of said second gating unit 15. The outputs of said first gating unit 14 are applied via a group B of reading lines constituting a part of a group A of central lines to inputs/outputs of said control unit 11 and to outputs of said second gating unit 15.

The invented device determines in the course of a periodically repeated measuring procedure the limited minimum and the limited maximum of time intervals between two signal changes (these two signal changes arriving not necessarily on the same input line, and one signal change not necessarily being immediately followed by the other). These two values (ie. limited minimum and maximum) are characteristic of both data transmission rate and signal distortion. (That is; difference of the exact bit time and the minimum/maximum value, related to the exact - nominal - bit

time and multiplied by 100 is equal to the negative/positive bit time deviation - jitter - expressed in percentage of the nominal bit time. By defining various minimum and maximum limit values the jitter of signal edges being at various bit distances relative to the given start signal edges can be examined and determined, if measuring is carried out by sections (see description of fig.1.). Into this case, said minimum/maximum limit value has to be suitably defined according to a relative time position being a half bit time less/greater than the probable position of the signal edge (for example the leading edge of the STOP-bit) to be examined. If measuring is to be made continously, said minimum/maximum limit value is to be chosen according to 0,5/1,5 theoretical bit time. If at the beginning of the measurement not even the transmission rate (that is: the theoretical bit time) is known, at first continuous measuring mode has to be selected, and baud-rate is to be determined, by symply chosing value of minimum limit=0. Value of maximum limit is in this case of no importance. Transmission rate can be calculated on the basis of the measured minimum value. Thereafter, either continuous or sectioned measuring mode can be selected, and signal distortion can be measured and calculated as described above.

As can be seen, it is of a great importance, that values of said minimum and maximum limits be chosen appropriately.

In said device according to figure 2., said minimum and maximum limit values can programmably be loaded into said baud-rate and signal distortion detector unit 12, via said group C of writing lines. If a signal is generated by said address decoder unit 13 onto said first addressing line b, said minimum limit value will be loaded, and so it will be equal with data being present on said group C of writing lines.

If a signal appears on said second addressing line d, data being present on said group C of writing lines will be stored as value of said maximum limit. Operation of said address decoder unit 13

is controlled by said control unit 11 via said D group of address and control lines.

As a result of a number of periodical measuring sequences, on appropriate outputs of said baud-rate and signal distortion unit will appear a value representing the measured minimum value (first bunch F of data lines) and the measured maximum value (second bunch C of data lines). As a result of a pulse, generated by said address decoder unit 13 and appearing on said third addressing line e, data being present on said first bunch F of data lines will be gated by said first gating unit 14 onto said group B of reading lines, being a subset of said group A of central lines, then may then be processed by said control unit 11), and thereafter the actual minimum value will be set to the theoretical maximum in said baud-rate and signal distortion detector unit 12. As a result of another pulse also generated by said address decoder unit 13 and appearing on said fourth addressing line f, data being present on said second bunch G of data lines will be gated by said second gating unit 15 onto said group B of reading lines, being a subset of said group A of central lines (they may then be processed by said control unit 11), and thereafer the actual maximum value will be set to the theoretical minimum in said baud-rate and signal distortion detector unit 12.

Operation of a preferred embodiment of said baud-rate and signal distortion detector unit 12 of the invention will be explained with respect to fig.3.

Said baud-rate and signal distortion detector unit 12 comprises a time marker circuit 16, a counter 17, a minimum limit register 18, a maximum limit register 19, a first comparator circuit 20, a second comparator circuit 21, a third comparator circuit 22, a fourth comparator circuit 23, a first gating circuit 24, a limited minimum register 25, a second gating circuit 26 and a limited maximum register 27.

The inputs of said time marker circuit 16 are connected to a group E of input data lines, another input of it is connected via a third transit line t to an input of said first gating circuit 16 and to the output of said first comparator circuit 20. The outputs of said time marker circuit 16 are applied via an enabler line i to an input of said counter 17, via a reset line s to another input of said counter 17, via a write line h to another input of said first gating circuit 24 and to an input of said second gating circuit 26, respectively. A further input of said counter 17 is connected to a synchronizer line g, constituting part of a group A of central lines. The outputs of said counter 17 are applied via a group H of internal data lines to inputs of said first, second, third and fourth comparator circuit (20, 21, 22, 23), furthermore to inputs of said limited minimum register 25 and to those of said limited maximum register 27. The inputs of said minimum limit register 18 are connected partly to a first addressing line b, partly, via a group Q of data lines being a subset of a group A of central lines to inputs of said maximum limit register 19. The outputs of said minimum limit register 18 are applied via a first group J of transit lines to further inputs of said first comparator circuit 20. A further input of said maximum limit register 19 is connected to a second addressing line d, its outputs are applied via a second group K of transit lines to further inputs of said second comparator circuit 21. A further input of said first gating circuit 24 is applied via a fifth transit line v to the output of said third comparator circuit 22, its output is connected via a first transit line k to a further input of said limited minimum register 25. Further input of said limited minimum register 25 is connected to a third addressing line, its outputs are connected via a first bunch F of data lines to further inputs of said third comparator circuit 22. Further inputs of said second gating circuit 26 are connected via a fourth transit line u to the output of said second comparator circuit 21, and via a sixth transit line y to the output of said fourth comparator circuit 23, respectively. The output of said second gating circuit 26 is applied via a second transit line m to an input of said limited

maximum register 27. A further input of said limited maximum register 27 is connected to a fourth addressing line f, its outputs are connected to a second bunch G of data lines, and via second bunch G of data lines to further inputs of said fourth comparator circuit 23.

Said minimum limit register 18 will be loaded with data being present on group Q of data lines by a pulse arriving on first addressing line b. Data being stored in such a way in said minimum limit register 18 (that is: the actual minimum limit) appears on its outputs, that is on said first group J of transit lines, and on inputs of said first comparator circuit 20. Said maximum limit register 19 will be loaded in a similar way with data being present on group Q of data lines by a pulse arriving on second addressing line d. Data being stored in such a way in said maximum limit register 19 appears on its outputs, that is on said second group K of transit lines, and will also be present on inputs of said second comparator circuit 21. As on effect of the input data stream arriving on said group E of input data lines, said time marker circuit 16 will generate pulses on its outputs, and these pulses will reach via said enabler line i and reset line s the inputs of said counter 17, and via said write lines h the inputs of said first gating circuit 24 and second gating circuit 26. When a pulse arrives on said reset line s, said counter 17 will be cleared (set to zero), and as an effect of a pulse applied to said enabler line i; said counter 17 will be enabled, that is, in its enabled state, contents of said counter 17 will be incremented (the counter will count up) whenever a pulse arrives on said synchronizer line g. Said first comparator circuit 20 will generate a logical 1 state on its output, if the value being present on outputs of said counter 17 is greater than that of the outputs of said minimum limit register 18. In a similar way, said second comparator circuit 21 will show a logical 1 state on its output, whenever value on outputs of said counter 17 is less than value on outputs of said maximum limit register 19. Said minimum limit register 25 holds always the previously stored limited minimum value, and in a similar way said limited maximum register 27 contains the

limited maximum value previously stored. Said third comparator circuit 22 will present on its output a logical 1 level, whenever value on outputs of said counter 17 is less than the previously stored limited minimum value, represented by the outputs of said limited minimum register 25. Value on output of said fourth comparator circuit 23 will be a logical 1, every time the value represented by outputs of said counter 17 is greater than the previously stored limited maximum value, represented by outputs of said limited maximum register 27. Said first gating circuit 24 will generate a pulse on its output concurrently with any pulse arriving on said write line h, if said first comparator circuit 20 and third comparator circuit 22 concurrently have logical 1 states on their outputs during the pulse arriving on said write line h. The pulse arriving on said first tarnsit line k, being generated by said first gating unit loads said limited minimum register 25 with data being present on said group H of internal data lines, which represent the value of time interval measured (counted) between the last two examined signal changes. Contents of said limited minimum register, representing the previously stored limited minimum limit value, appear on said first F bunch of data lines. On said third addressing line e a pulse appears, when said control unit 11. (see fig.2) reads contents of said limited minimum register 25 by the help of said address decoder unit 13. The pulse arriving on said third addressing line e loads said limited minimum register with the maximum value that theoretically can be stored by the register (that is: all bits of said register will be set to logical 1).

Said second gating circuit 26 will generate a pulse on its output concurrently with any pulse arriving on said write line h, if said second comparator circuit 21 and fourth comparator circuit 23 concurrently have logical 1 states on their outputs during the pulse arriving on said write line h. The pulse generated by said second gating circuit 26 and appearing on said second transit line m loads said limited maximum register 27 with data being present on said group H of internal data lines, which as mentioned above, represent the value of time interval measured (counted) between the last two examined signal changes. Contents of said limited maximum register, representing the previously stored limited

maximum value, appear on said second bunch G of data lines. Said limited maximum register 27 will be cleared (all bits of said limited maximum register 27 will be set to zero, that is to the minimum absolute value, that can be stored by it), if a pulse arrives on said fourth addressing line f. (On said fourth addressing line f a pulse appears, when said control unit 11 - see fig.2. - reads contents of said limited maximum register 27.) In such a way, if measuring lasted long enough, said limited minimum register 25 and said limited maximum register 27 will hold minimum and maximum values, statistically characterizing the input data stream arriving on said group E of input data lines.

Operation of a possible, simple embodiment of said time marker circuit 16 will also be explained with respect to fig 3. Said time marker circuit 16 is in this case a signal change indicator circuit constituted by edge-triggered monostable multivibrators. In this case, said group E of input data lines is represented by a single input line, on which input data arrive. After every signal change (signal edge) said signal change indicator circuit 16 generates two successive pulses. First it gives a pulse onto said write line h, and thereafter another one concurrently onto said reset line s and said enabler line i. In this case, said third transit line, connected to said time marker circuit 16 is of no importance.

A possible embodiment of said time marker circuit 16 will be described with respect to fig. 4.

In this embodiment, said time marker circuit 16 includes a first signal change indicator circuit 28, a second signal change indicator circuit 29 and a storage 30.

The inputs of said first signal change indicator circuit 28 comes from a first input data line n, being part of said group E of input data lines, its output is applied via a transit data line r to the input of said storage 30. The input of said second signal change indicator circuit 29 is connected to a second input data line p, also being part of said group E of input data lines, the

outputs of said second signal change indicator circuit is partly connected via said reset line s to a further input of said storage 30, partly to said write line h, respectively. The output of said storage 30 is applied to said enabler line i.

In this case, said group E of input data lines consist of two lines. These two lines are: first input data line n and second input data line p. Said first signal change indicator circuit 28 gives a pulse onto said transit data line r after every signal change occuring on said first input data line n. Said second signal change indicator circuit 29 gives a pulse onto said reset line s and said write line h after every signal change occuring on said second input data line p. Said storage 30 is set to logical 1 state, and gives a logical 1 onto said enabler line i, whenever a pulse arrives on said transit data line r; it will be cleared (set to zero) and gives a logical 0, whenever a pulse arrives on said reset line s.

By using the above embodiment of said time marker circuit, the minimum/maximum values of time distances between signal changes on two different signal lines (for example: synchron clock and data line in case of a synchronous serial input data stream) can be determined. In this way signal skew can be determined.

Another preferred embodiment of said time marker circuit will be explained with respect to fig. 5.

According to this embodiment, said time marker circuit 16 comprises a signal change and start/stop bit indicator circuit 31 and a bistable multivibrator 32. The input of said signal change and start/stop bit indicator circuit 31 is connected to an input data line o, being part of said group E of input data lines, its outputs are connected partly via a reset line s to an input of said bistable multivibrator 32, partly via a stop signal line q to another input of said bistable multivibrator 32 and partly to said write line h, respectively. The output of said bistable multivibrator is connected to said enabler line i.

In this case, said group E of input data lines consists of a single input data line o. Via this input data line o a serial data stream arrives and given to the input of said signal change and start/stop bit indicator circuit 31. When said signal change and start/stop bit indicator circuit 31 detects a START bit, on the first (leading) edge of the START bit it gives a pulse onto said reset line s. When said signal change and start/stop bit indicator circuit detects a STOP-bit (that is, it detects a 0→1 signal change in an appropriate neighbourhood of the probable position of the leading edge of the STOP bit; this o→1 change will only occur, when STOP bit is preceeded by a bit, having a value of logical 0 in the data stream), it gives a pulse onto said stop signal line q. If said signal change and start/stop bit indicator circuit 31 detects any other signal changes between respective START and STOP signal edges, it gives a pulse onto said write line h on every appropriate signal change. Said bistable multivibrator 32 will be set to logical 1 state, and will give a logical 1 signal onto said enabler line i, whenever a pulse arrives on said reset line s. Said bistable multivibrator 32 will be cleared, and will give a logical 0 signal onto said enabler line i, when a pulse arrives on said stop signal line q. Said third transit line t, shown in fig. 3 is in this embodiment of no importance. A further preferred embodiment of said time marker circuit 16 will be described with respect to fig. 6.

In this embodiment, said time marker circuit 16 comprises a signal change and start bit indicator circuit 33, a bistabil multivibrator circuit 34 and on AND gate 35.

The input of said signal change and start bit indicator circuit is connected to said input data line o, being part of said group E of input data lines, its outputs are connected partly to said reset line s, and via said reset line s to an input of said bistable multivibrator circuit 34, partly to said write line h, and via said write line h to an input of said AND-gate 35. Another input of said AND-gate 35 comes from said third transit line t, its output is connected via a stopping line z to another input of said bistable multivibrator circuit 34. The output of said bistable multivibrator circuit 34 is connected to said enabler line i.

In this case, said group E of input data lines consists of an input data line o. Said signal change and start bit indicator circuit monitors input signal stream arriving on said input data line o, and whenever it detects any signal change, it gives a pulse onto said write line h. Furthermore, if said signal change and start bit indicator circuit detects a START bit (that is: on leading edge of any START bit), it gives a pulse onto said reset line s, and in such a way it sets said bistable multivibrator circuit 34 to a logical 1 state. Thereafter , said bistable multivibrator 34 gives a logical 1 signal onto said enabler line i. Said bistable multivibrator circuit 34 will be cleared (that is: set to logical 0 state) when a pulse arrives on said stopping line z. Said AND gate 35 generates a pulse on its outputs, and gives this pulse onto said stopping line, when a pulse arrives on said write line h (generated by said signal change and start bit indicator circuit 33), and at the same time a logical 1 state is present on said third transit line t.

ADVANTAGES OF THE INVENTION

The advantages of the invented device and procedure can be summarized in the following:

a./ Data transmission rate and signal distortion may be determined by using the same method and same device.

2./ Data transmission rate may not only be determined at the beginning of the data transmission, if at first special predetermined characters are transmitted, but at any time during the data transmission, without any constraints with respect to the transmitted characters, supposing that within a limited time interval at least one character is transmitted in which a signal change will be followed by another within a time interval according to a single bit-time. This enables data transmission rate to be determined for example by signal- and protocol anlyzer devices, "listening to" a given

data channel in a discretional time interval.

3./ Determining signal distortion doesn't require signal regeneration.

4./ By applying the invented device and procedure input data signal can be analized in detail. When selecting continuous measuring mode, jitter of a single data bit can be determined; however if measuring by sections is selected, consequent frequency deviation can be determined at any time position relative to a given start signal edge. In case of a syhnchronous data transmission, phase deviation and skew between synchronous clock and data signal can also be determined.

5./ The invented device may be realized in a single LSI integrated circuit that may be programmed by a microprocessor.

C L a I M S

1. A procedure for determining data transmisson rate or signal distortion or both characteristic of serial data transmisson signals in the course thereof at first signal changes are indicated, then the time interval between two signal changes is determined and stored, characterised in that a time interval measured last is compared with a previously stored minimum value and at the same time with a minimum limit postulated and stored beforehand; the value of time interval just measured will only be stored as a new minimum value, if it is less than said previously stored one, but at the same time it is greater than said postulated minimum limit; and optionally in the course of the comparisons it will be investigated , whether the value last measured is greater than a previously stored maximum value, and at the same time, it is less than a maximum limit postulated and stored beforehand, and the new value will only be stored as a new maximum value, if the above conditions are fulfilled.

2. Said procedure according to claim 1, w h e r e i n at the beginning of a measuring sequence said previously stored minimum value is preset to a theoretical defined initial maximum and said optionally considered and previously stored maximum value is preset to a theoretically defined initial minimum value.

3. A device at determining data transmission rate and/or signal distortion of serial data transmission signals, particularly to realize procedure according to claims 1,2, which comprises a control unit, an address decoder unit, a baud-rate detector unit and a first gating unit, each connected to a grou p A of central lines, w h e r e i n the said baud-rate detector is a continoued baud-rate detector and signal distortion detector unit (12), and said device comprises further a second gating unit (15); and inputs of said baud-rate and signal distortion detector unit (12) are connected via a first addressing line (b) and via a second addressing line (d) to respective outputs of said address decoder unit (13), another input via a third addressing line (e) to a further output of said address decoder unit (13) and to an input of said first

gaint unit (14), a further input via a fourth addressing line (f) to a further output of said address decoder unit (13) and to an input of said second gating unit (15), further inputs of it to a group (E) data lines constituting an input of the device; furhter input via a group (C) of writing lines being a subset of a group (A) of central lines to inputs/outputs of said control unit (11); outputs of said baud-rate and signal distortion detector unit (12) via a first bunch (F) of data lines to further inputs of said first gating unit (14) via a second bunch (G) of data lines to further inputs of said second gating unit (15); outputs of said first gating unit (14) are applied via a group (B) of reading lines constituting a part of a group (A) of central lines to inputs/outputs of said control unit (11) and to outputs of said second gating unit (15). (Fig. 2)

4. A device, according to claim 3, w h e r e i n said baud-rate and signal distortion detector unit (12) comprises a time marker circuit (16), a counter (17), a minimum limit register (18), a maximum limit register (19), a first comparator circuit (20), a second comparator circuit (21), a third comparator circuit (22), a fourth comparator circuit (23), a first gating unit (24), a limited minimum register (25), a second gating circuit (26) and a limited maximum register (27): inputs of said time marker circuit (16) are connected to said group (E) of input lines, another input of said time marker circuit (16) is connected via a third transit line (t) to an input of said first gating circuit (24) and to an output of said first comparator circuit (20): outputs of said time marker circuit (16) are applied via an enabler line (i) to aninput of said counter (17), via a reset line (s) to another input of said counter (17), via a write line (h) to another input of said first gating circuit (24) and to an input of said second gating corcuit (26), respectively; a further input of said counter (17) is connected to a synchronizer line (g), constituting part of said group (A) of central lines; outputs of said counter (17) are applied via group (H) of internal data lines to inputs of said first, second, third and fourth comparator circuit (20,21,22, 23), furthermore to inputs of

said limited minimum register (25) and to those of said limited maximum register (27); inputs of said minimum limit register (18) are connected partly to said first addressing line (b), partly via group (Q) of data lines being a subset of said group (A) of central lines to inputs of said maximum limit register (19); outputs of said minimum limit register (18) are applied via a first group (J) of transit lines to further inputs of said first comparator unit (20); a further input of said maximum limit register (19) is connected to said second addressing line (d), its outputs are applied via a second group (K) of transit lines to further inputs of said second comparator circuit (21); a further inpu t of said first gating circuit (24) is connected via a fifth tranist (v) to an output of said third comparator circuit (22), its output is connected via a first transit line (k) to a further input of said limited minimum register (25); a further input of said limited minimum register (25) is connected to said third addressing line (e); its outputs are connected via said first bunch (F) of data linest o further inputs of said third comparator circuit (22); furhter imputs of said second gating circuit (26) are connected via a forth transit line (u) to an output of said second comparator circuit (21), and via a sixth transit line (y) to an output of said forth comparator circuit (23) respectively; an output of said second gating circuit (26) is applied via a second transit line (m) to an input of said limited maximum register (27); a further input of said limited maximum register (27) is connected to said fourth addressing line (f); it s outputs are connected to said second bunch (G) of data lines, and via said second bunch (G) of data lines to further inputs of said fourth comparator circuit (23). (Fig. 3)

5. A device according to claim 4, w h e r e i n said time marker circuit (16) is a signal change indicator circuit, suitably consisting of edge-triggered monostable multivibrators (Fig. 3).

6. A device according to claim 4, w h e r e i n said time marker circuit (16) includes a first signal change indicator circuit

(28), a second signal change indicator circu it (29) and a storage (30); an input of said first signal change indicator circuit (28) comes from a first input data line (n), being part of said group (E) of input data lines, its outputs is applied via a transit data line (r) to an input of said storage (30), an input of said second signal change indicator circuit (29) is connected to a second input data line (p) also being part of said group (E) of input data lines, while outputs of said second signal change indicator circuit are partly connected via said reset line (s) to a further input of said storage (30), partly connected to said write line (h); an output of said storage (30) is applied to said enabler line (i) (Fig. 4).

7. A device according to calim 4, w h e r e i n said time marker circuit (16) comprises a signal change and start/stop bit indicator circuit (31) and a bistable multivibrator (32) wherein an input of said signal change and start/stop bit indicator circuit (31) is connected to an input data line (o) being part of said group (E) of input data lines, outputs thereof are connected partly via said reset line (s) to an input of said bistable multivibrator (32), partly via a stop signal line (q) to a further input of said bistable multivibrator (32), and partly to said write line (h), while an output of said bistable multivibrator (32) is connected to said enabler line (i). (Fig.5)

8. A device, according to claim 4, w h e r e i n said time marker circuit (16) comprises a signal change and start bit indicator circuit (33), a bistable multivibrator circuit (34) and an AND-gate (35); an input of said signal change and start bit indicator circuit (33) is connected to an input data line (o) being part of said group (E) of input data lin es; outputs of said signal change and start bit indicator circuit (33) are connected partly to said reset line(s) and via said rese t line (s) to ain input

of said bistable multivibrator circuit (34) and partly to said write line (h) and via said write line (h) to an input of said AND-gate (35); another input of said AND-gate (35) comes from said third transit line (t); its output is c onnected via a stopping line (z) to another input of said bistable multivibrator circuit (34), while an output of said bistable multivibrator circuit is connected to said enabler line (i). (Fig. 6)

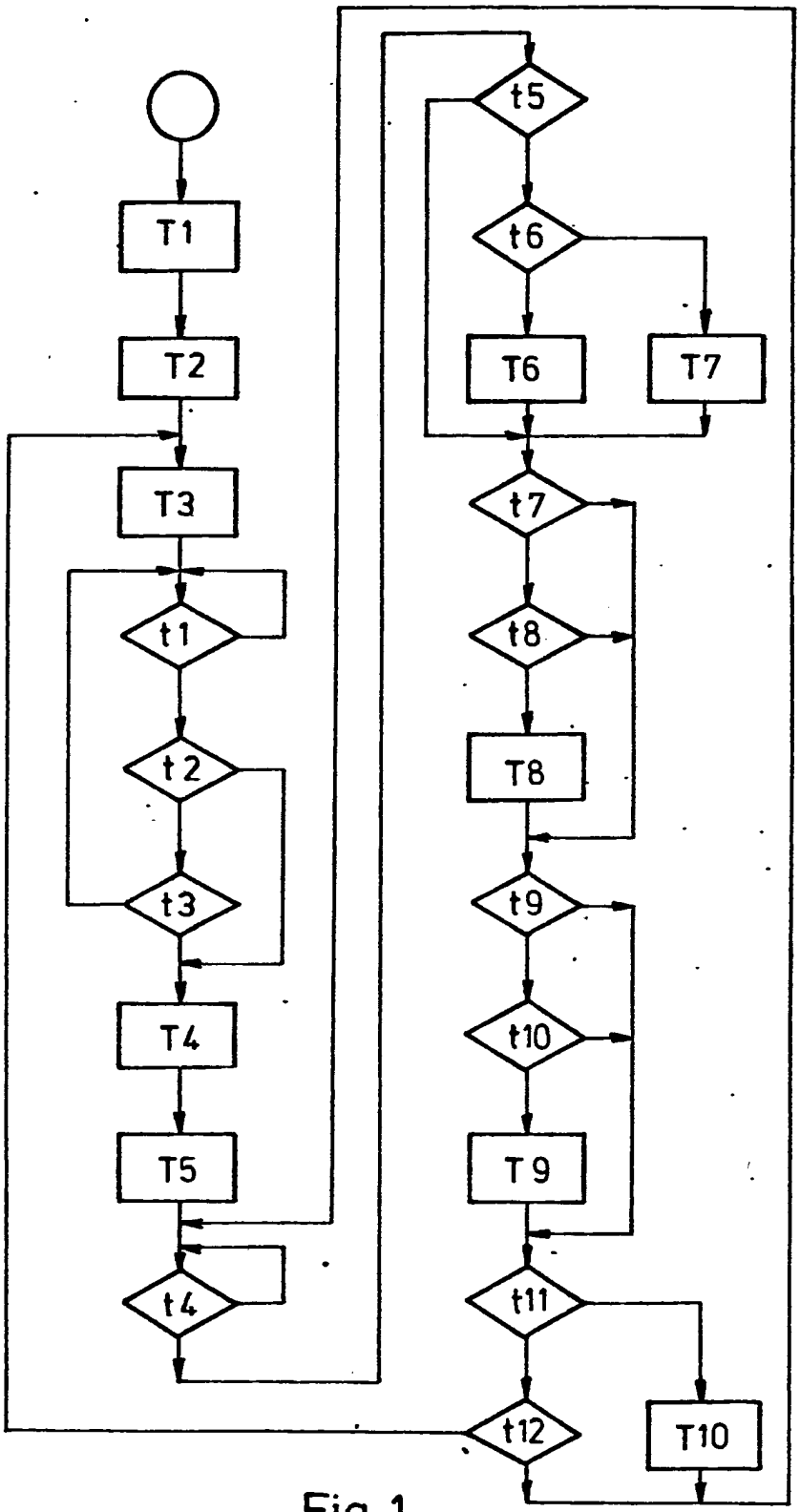

Fig.1

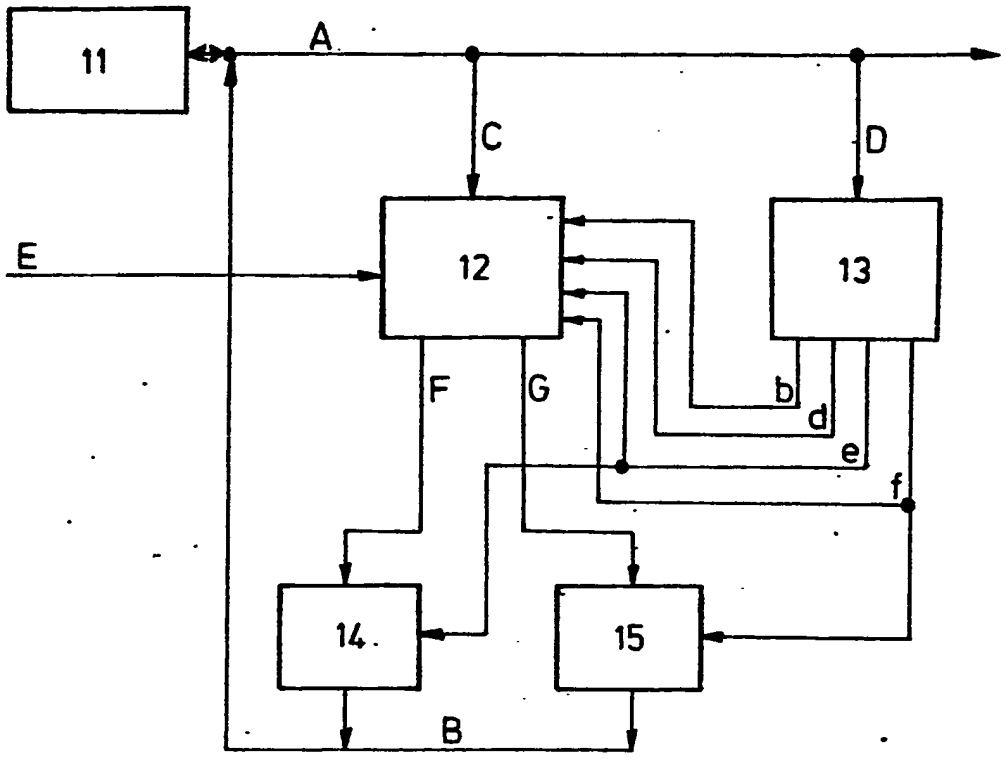

Fig. 2

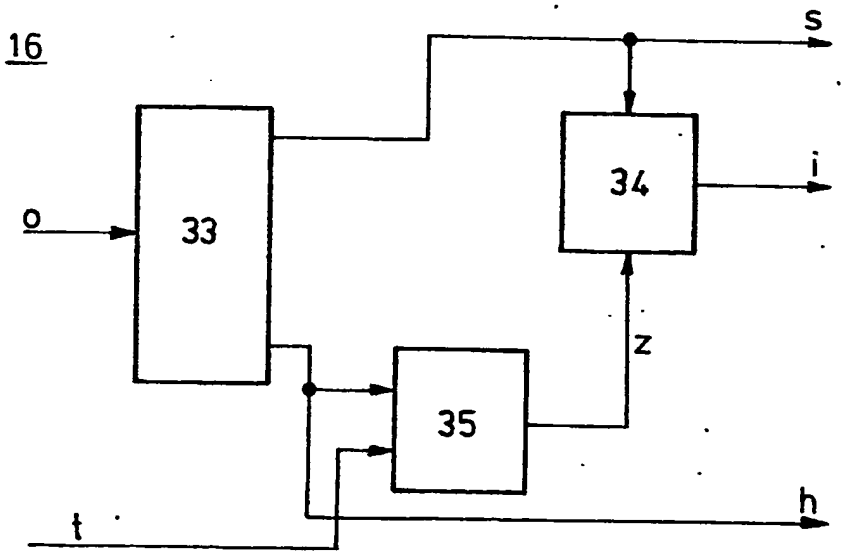

Fig.6

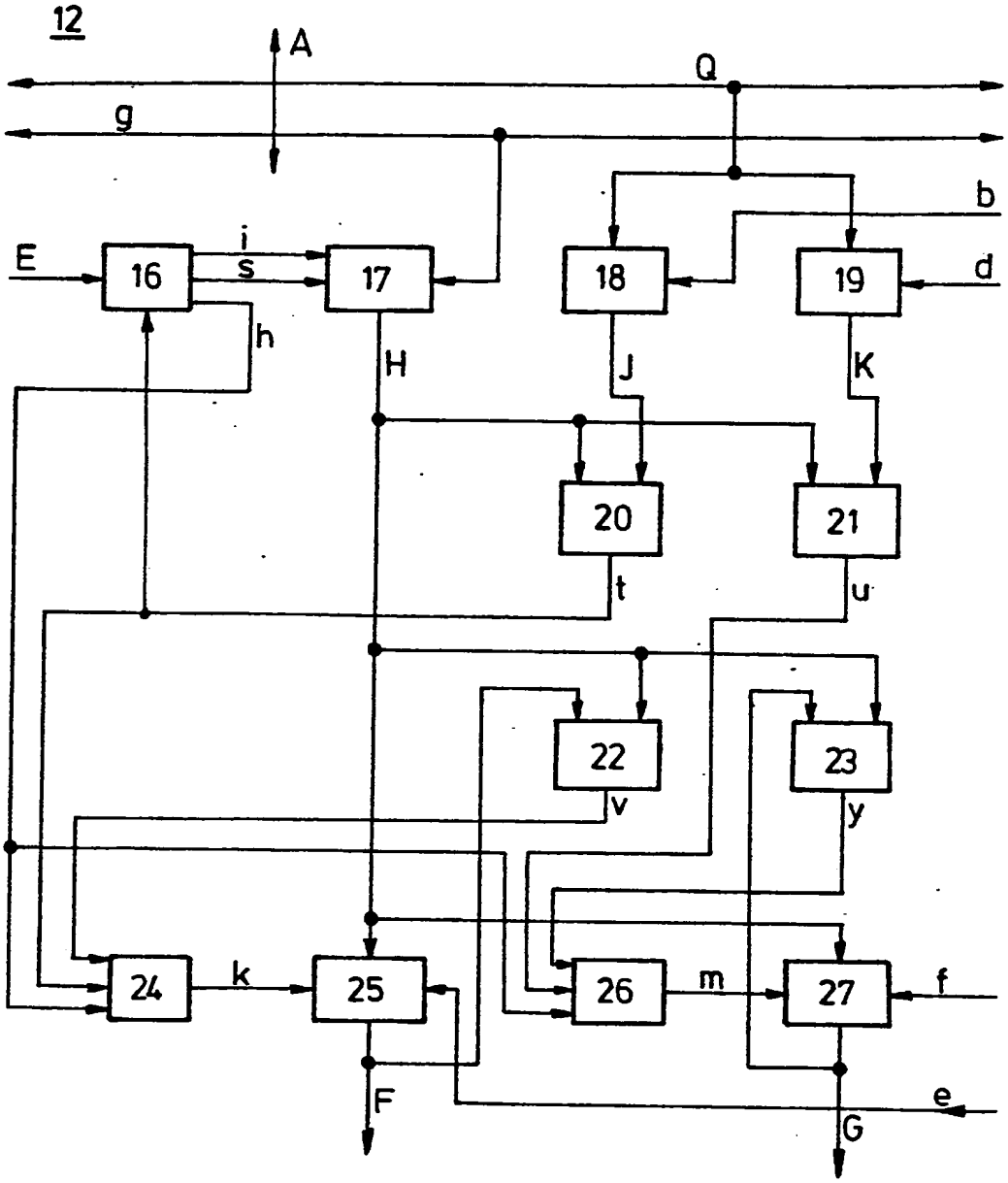

Fig.3

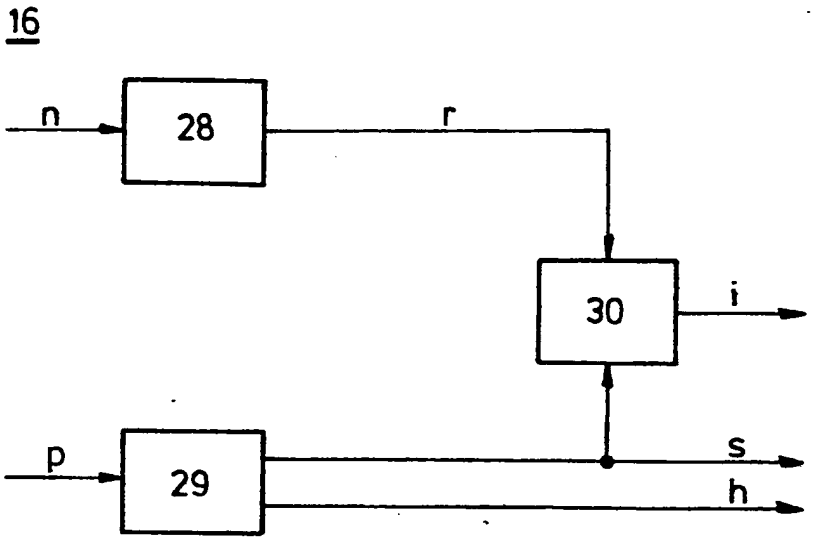

Fig.4

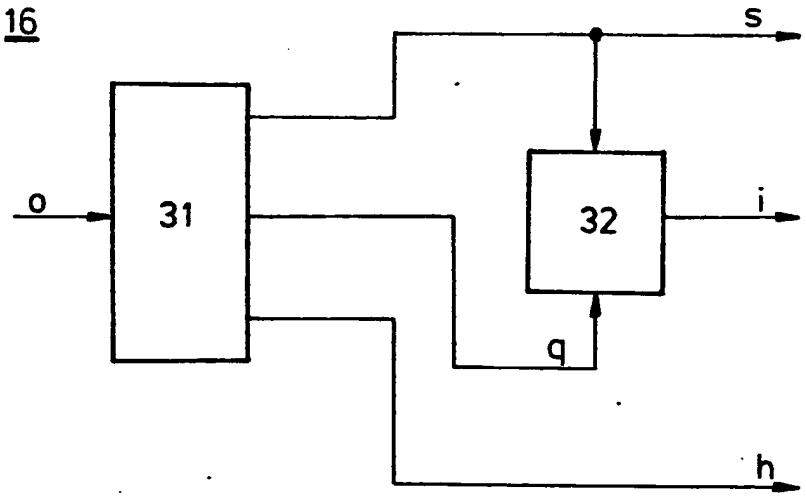

Fig.5

INTERNATIONAL SEARCH REPORT

International Application No PCT/HU 86/00070

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 04 L 11/08,11/12,25/03

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
Int.Cl.[4]	H 04 L, G 06 F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	US, A, 3 985 955 (BLASS et al.) 12 October 1976 (12.10.76), see abstract; column 3, line 33 - column 4, line 2; fig. 1.	(1,3,4)
A	DE, A1, 2 940 271 (HIBEN) 16 April 1981 (16.04.81), see page 7, line 7 - page 8, line 3.	(1)
A	DE, B, 1 285 499 (SIEMENS) 19 December 1968 (19.12.68), see column 2, line 36 - column 5, line 19; fig. 2,3.	(1,3,4,7)
A	Soviet Inventions Illustrated, section R, week E37, 24 October 1979, Derwent Publications LTD. London, see SU 636-814 (PISKUN).	(1,3,4)

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* Special categories of cited documents: [14]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
05 March 1987 (05.03.87)	11 March 1987 (11.03.87)
International Searching Authority	**Signature of Authorized Officer**
AUSTRIAN PATENT OFFICE	Pippan

Anhang zum internationalen Recherchenbericht über die internationale Patentanmeldung Nr.

Annex to the International Search Report on International Patent Application No. PCT/HU 86/00070

Annexe au rapport de recherche internationale relatif à la demande de brevet international n°.

In diesem Anhang sind die Mitglieder der Patentfamilien der im obengenannten internationalen Recherchenbericht angeführten Patentdokumente angegeben. Diese Angaben dienen nur zur Unterrichtung und erfolgen ohne Gewähr.

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned International search report. The Austrian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

La présente annexe indique les membres de la famille de brevets relatifs aux documents de brevets cités dans le rapport de recherche internationale visé ci-dessus. Les renseignements fournis sont donnés à titre indicatif et n'engagent pas la responsabilité de l'Office autrichien des brevets.

Im Recherchenbericht angeführtes Patentdokument Patent document cited in search report Document de brevet cité dans le rapport de recherche	Datum der Veröffentlichung Publication date Date de publication	Mitglied(er) der Patentfamilie Patent family member(s) Membre(s) de la famille de brevets	Datum der Veröffentlichung Publication date Date de publication
US-A -3 985 955	12/10/1976	AT-A - 8 131/74	15/09/1976
		AT-B - 336 698	25/05/1977
		BE-A1- 822 515	22/05/1975
		CH-A - 580 816	15/10/1976
		DE-A1- 2 358 296	05/06/1975
		DE-B2- 2 358 296	26/05/1977
		DE-C3- 2 358 296	12/01/1978
		DK-A - 6 066/74	21/07/1975
		FR-A1- 2 252 713	20/06/1975
		GB-A - 1 479 053	06/07/1977
		IT-A - 1 025 775	30/08/1978
		JP-A2-50-084 122	07/07/1975
		LU-A - 71 320	20/08/1975
		NL-A - 7 415 060	26/05/1975
		SE-A - 7 414 576	23/05/1975
		SE-B - 394 562	27/06/1977
		SE-C - 394 562	06/10/1977
DE-A1-2 940 271	16/04/1981	None	
DE-B -1 285 499	19/12/1968	BE-A - 704 196	22/03/1968
		GB-A - 1 161 951	20/08/1969
		NL-A - 6 712 738	25/03/1968
		NL-B - 156 558	17/04/1978
		US-A - 3 581 009	25/05/1971
		BE-A4- 805 468	28/03/1974